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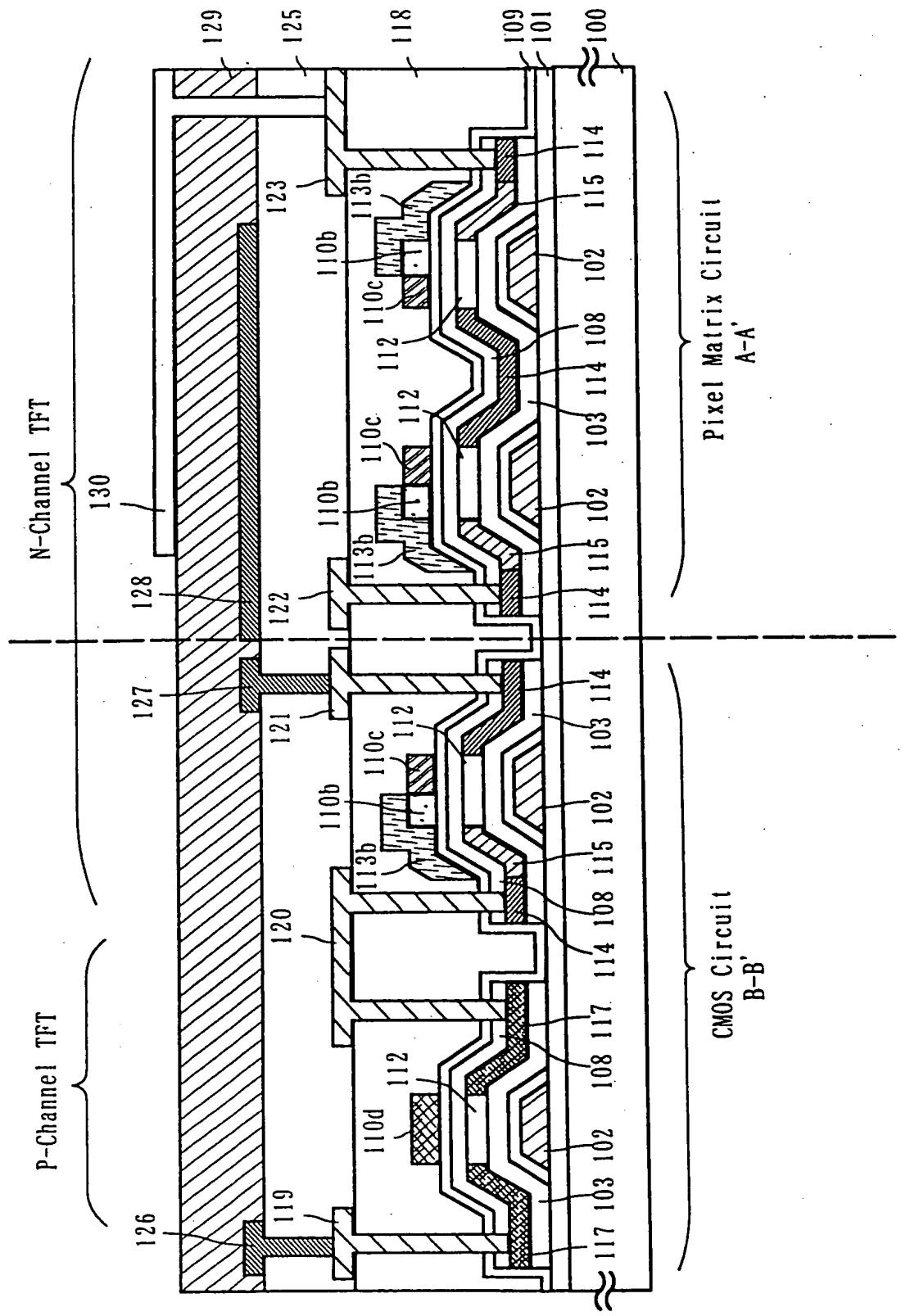
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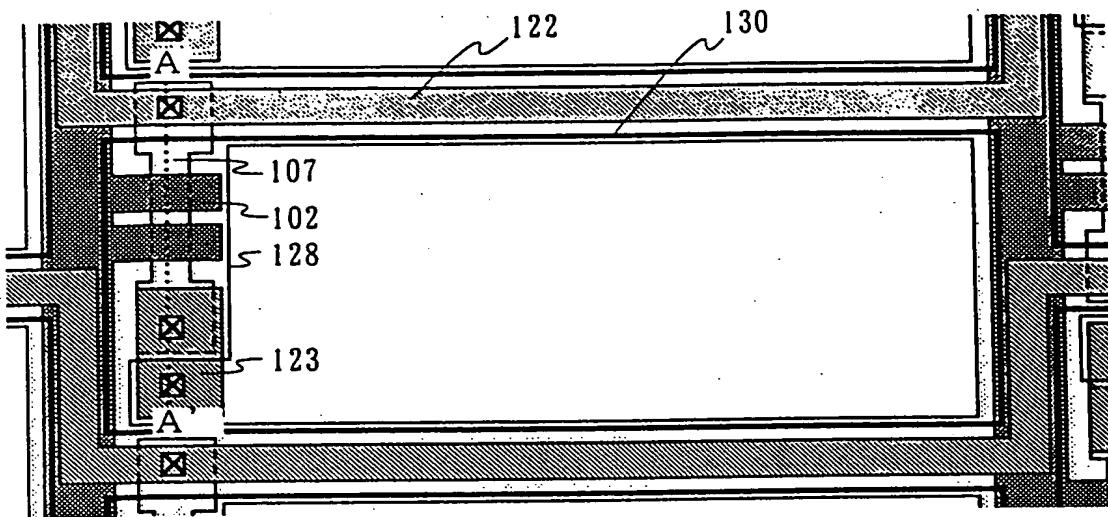


Fig. 2A

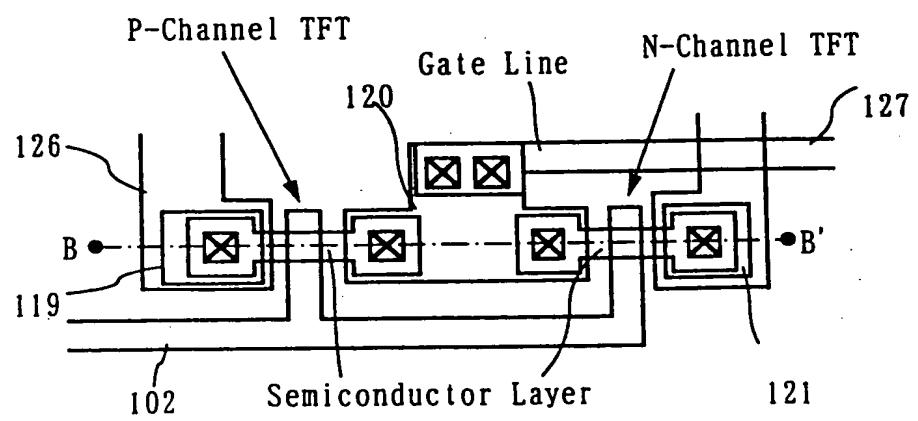


Fig. 2B

Fig. 3A

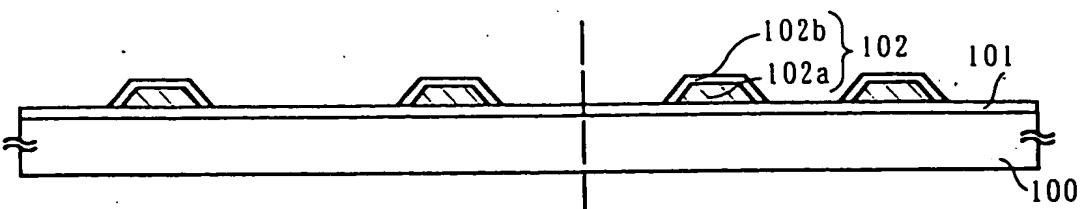


Fig. 3B

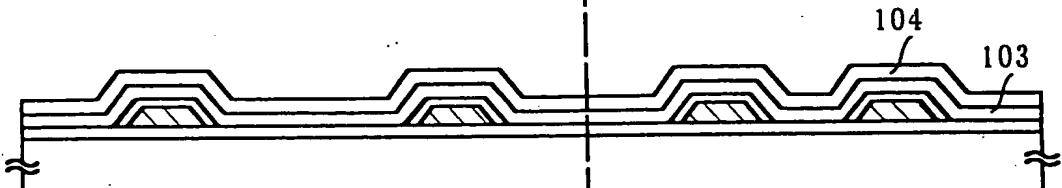


Fig. 3C

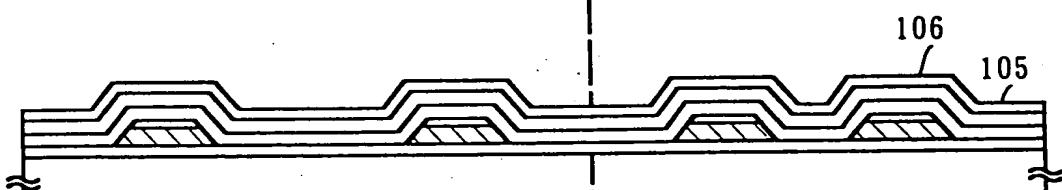


Fig. 3D

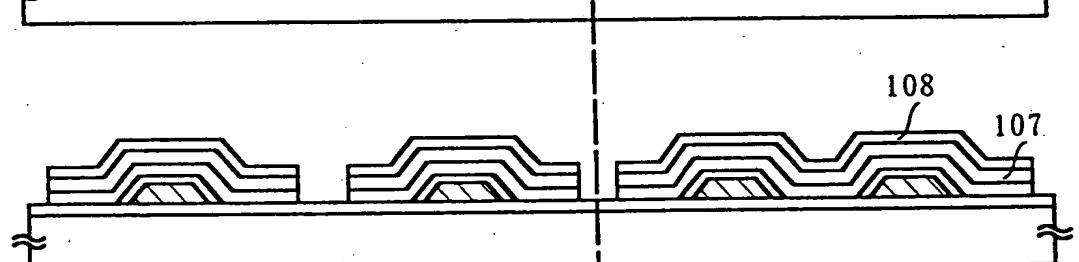


Fig. 3E

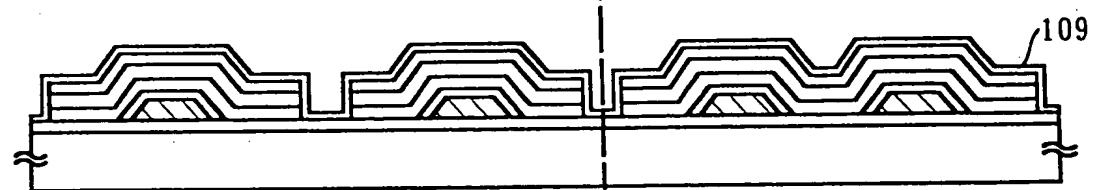
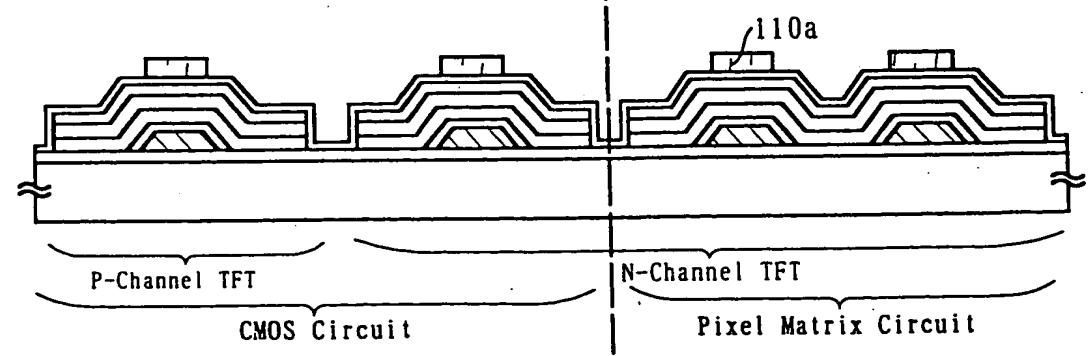
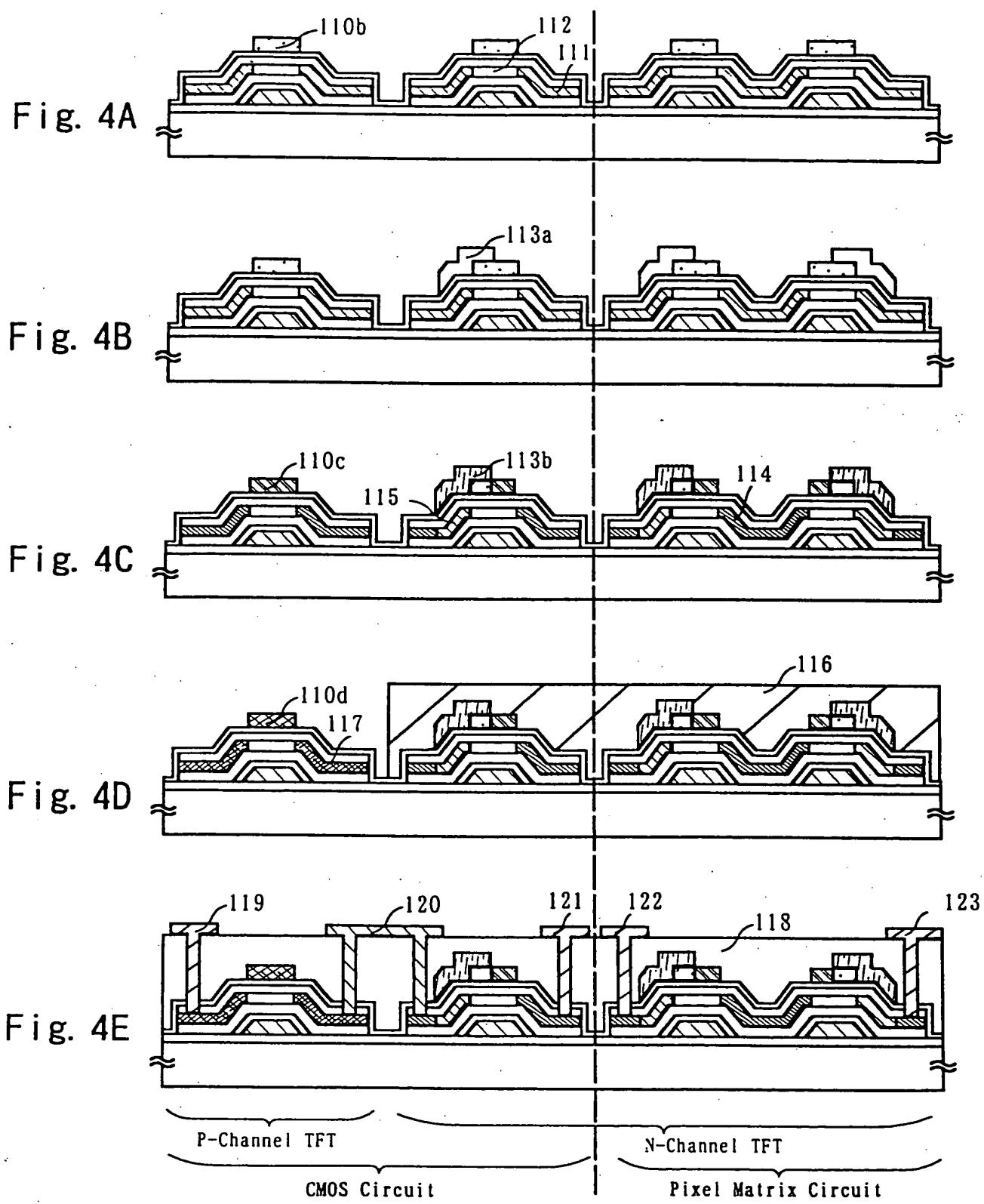


Fig. 3F



Pixel Matrix Circuit



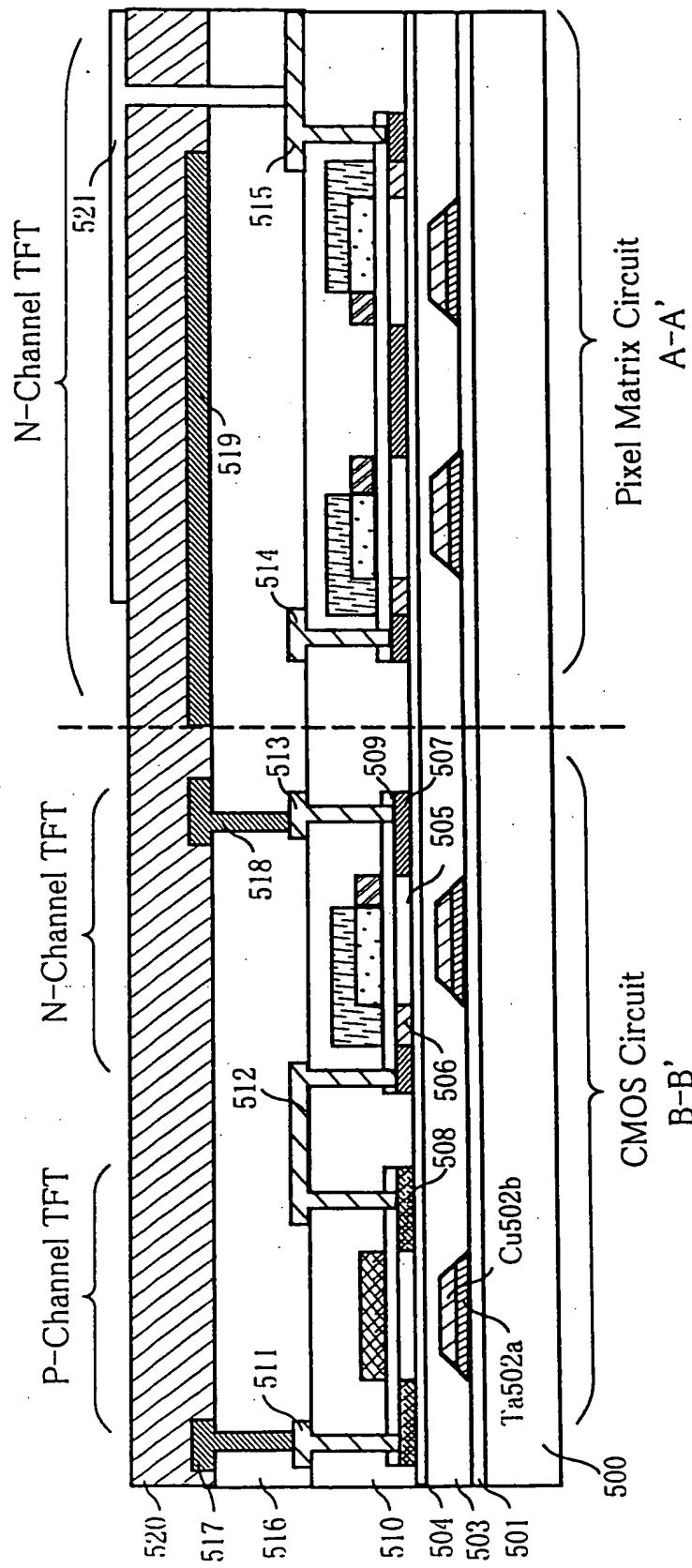


Fig. 5

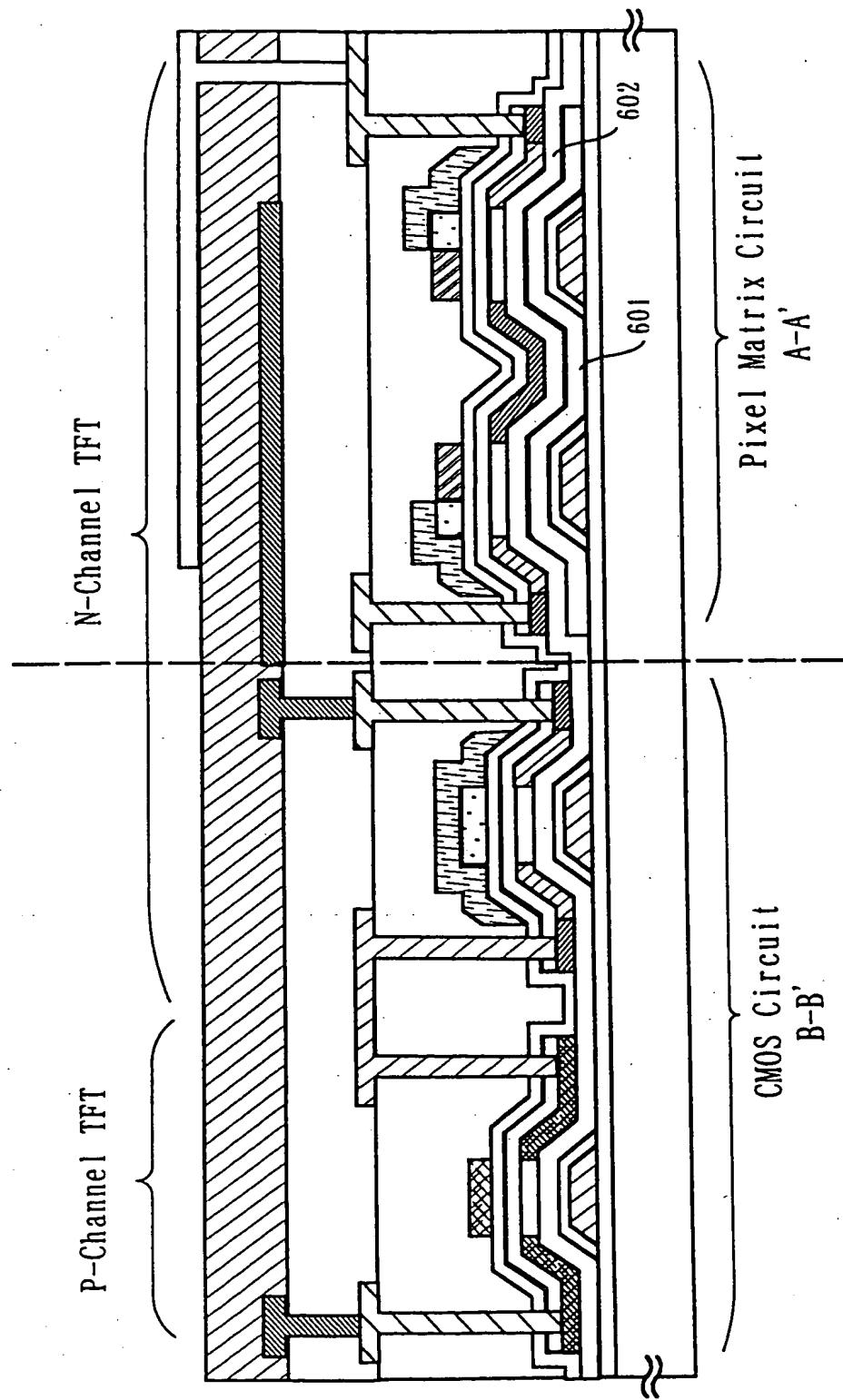
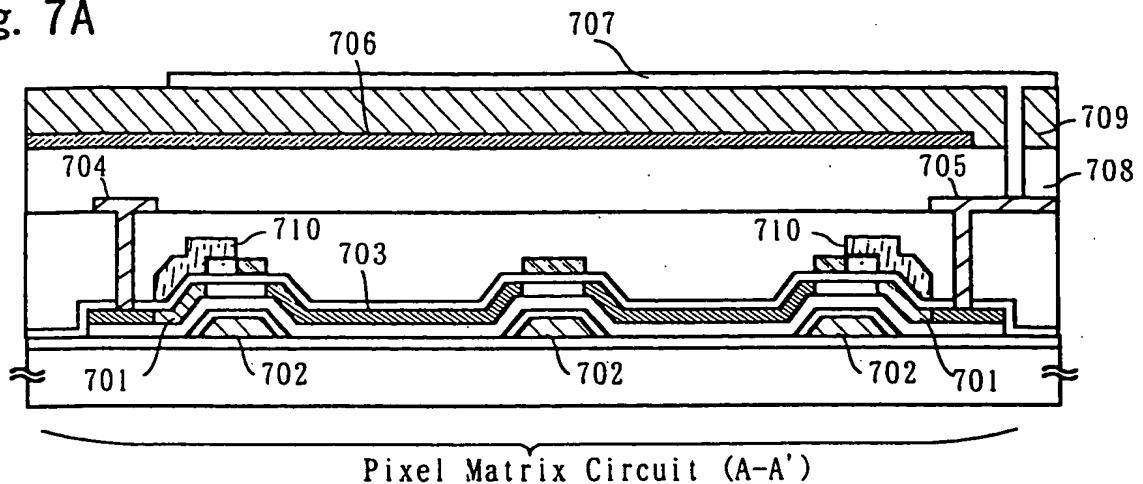


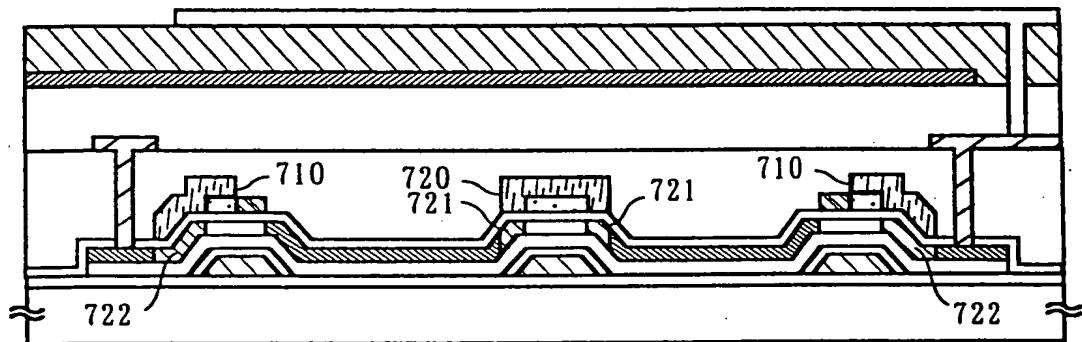
Fig. 6

Fig. 7A



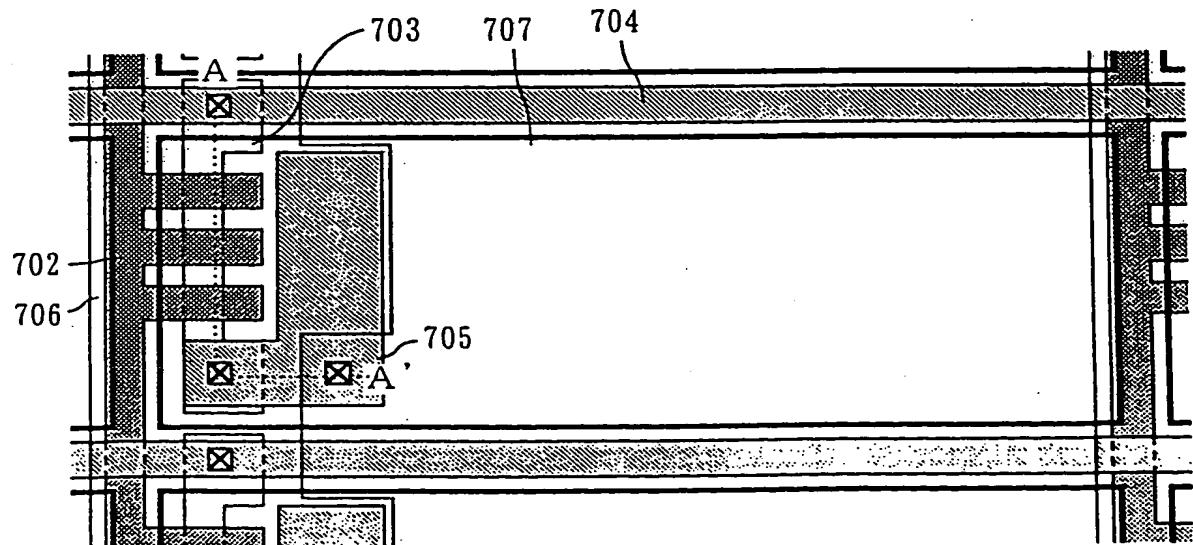
Pixel Matrix Circuit (A-A')

Fig. 7B



Pixel Matrix Circuit (A-A')

Fig. 7C



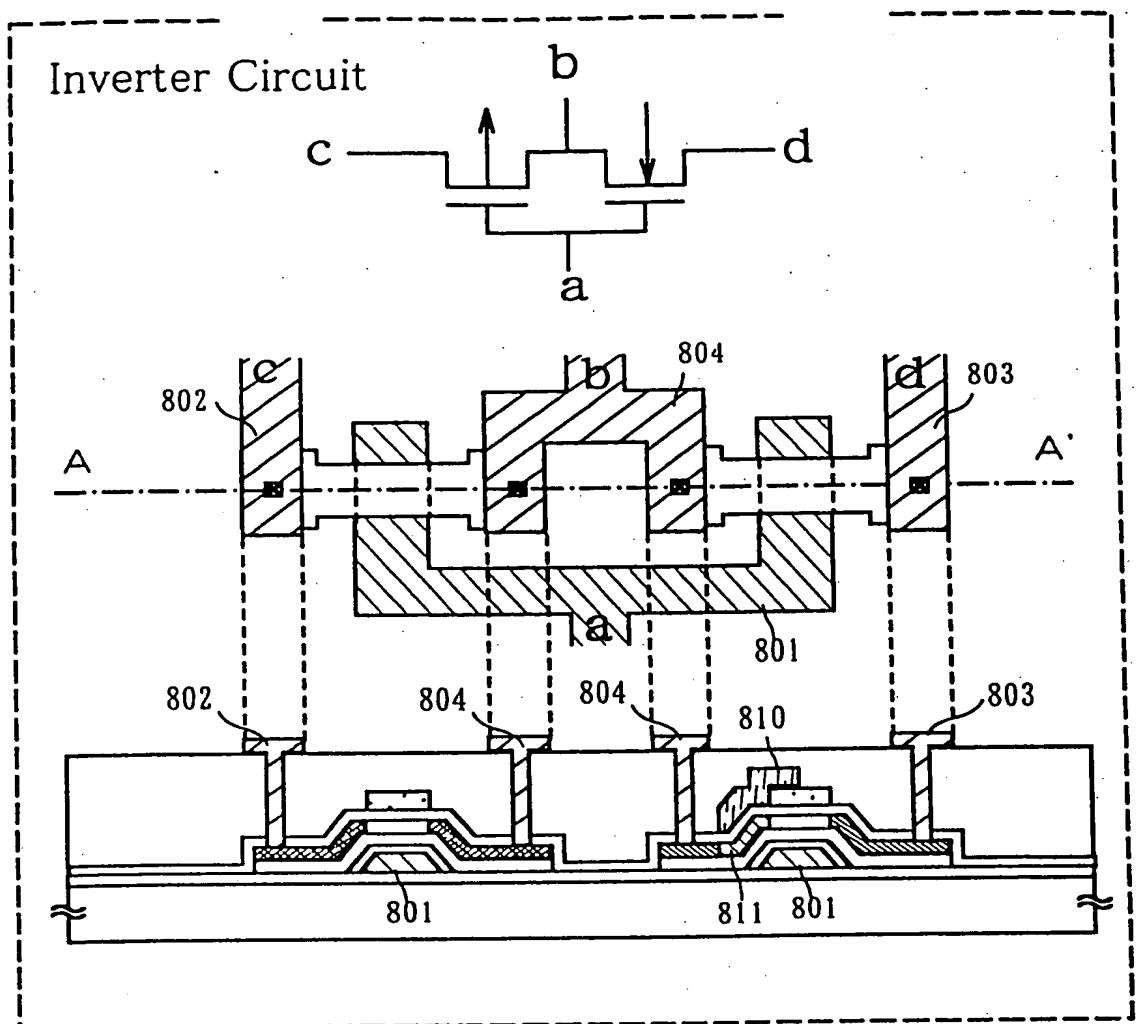


Fig. 8B

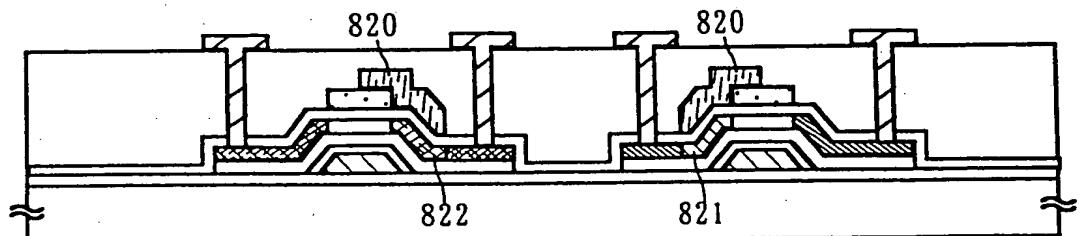
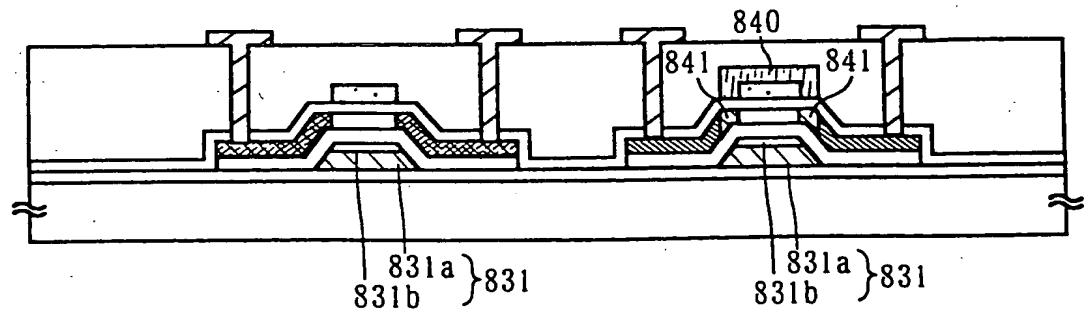


Fig. 8C



Buffer Circuit.

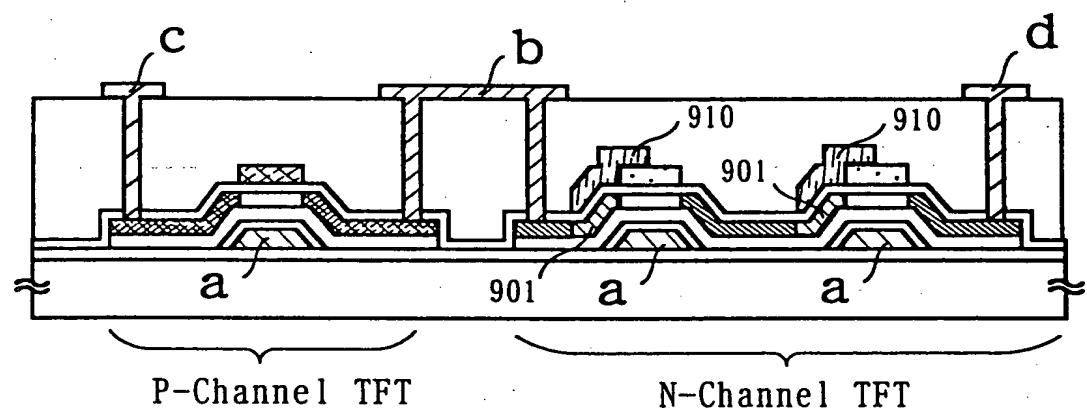
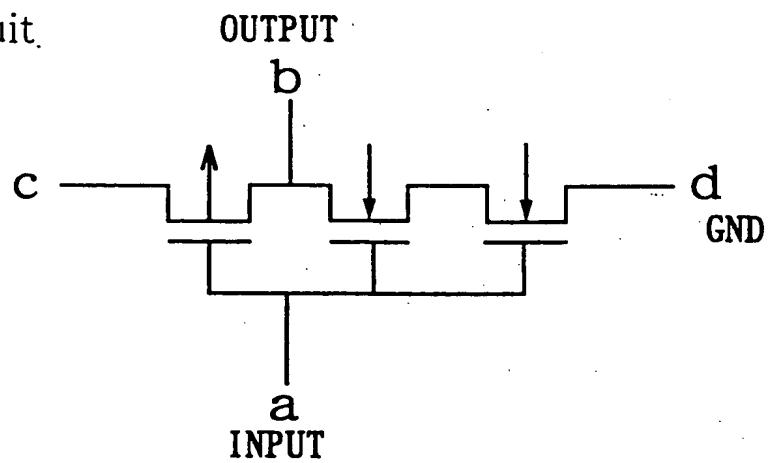


Fig. 9

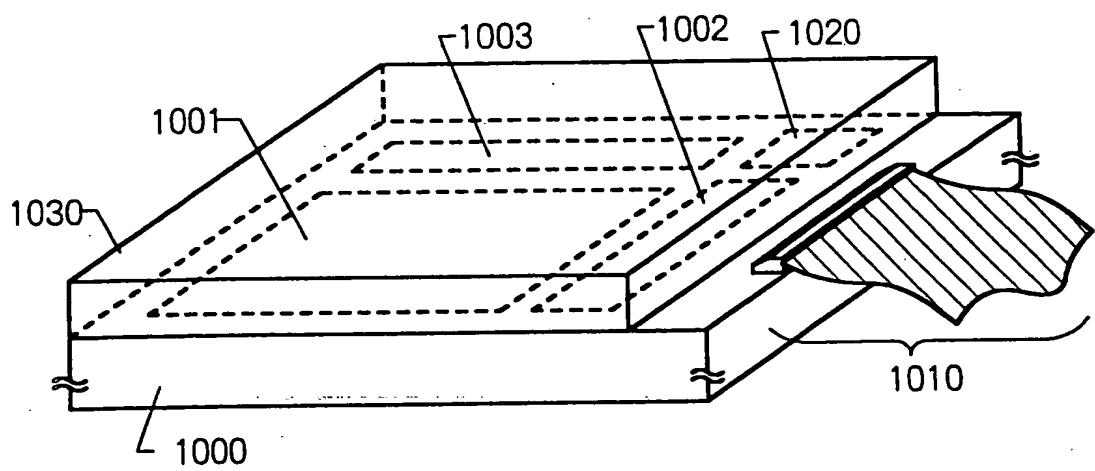


Fig. 10

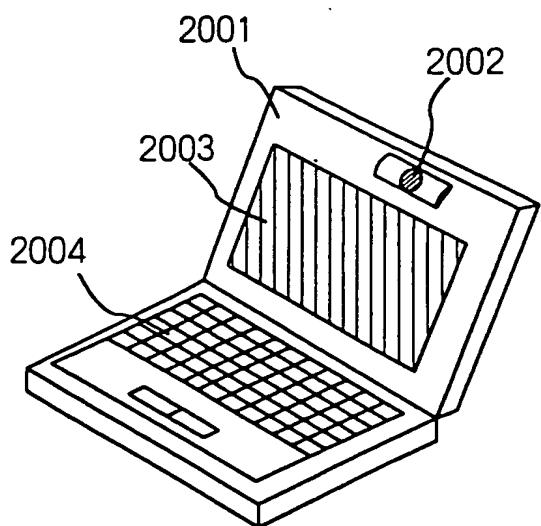


Fig. 11A

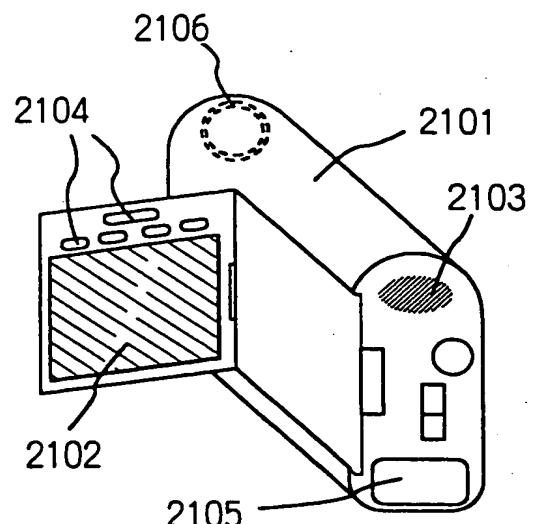


Fig. 11B

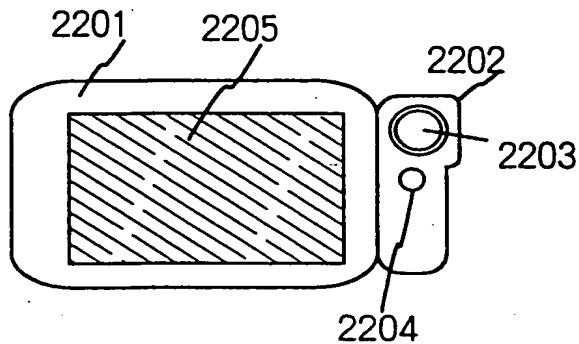


Fig. 11C

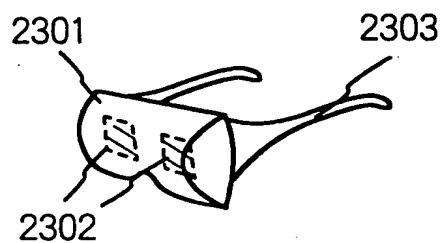


Fig. 11D

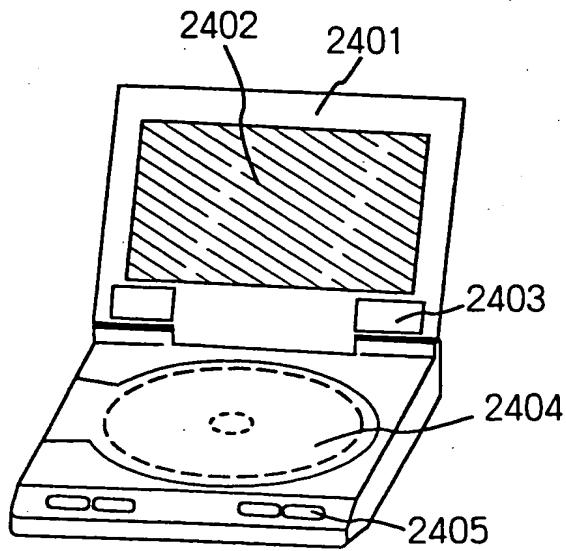


Fig. 11E

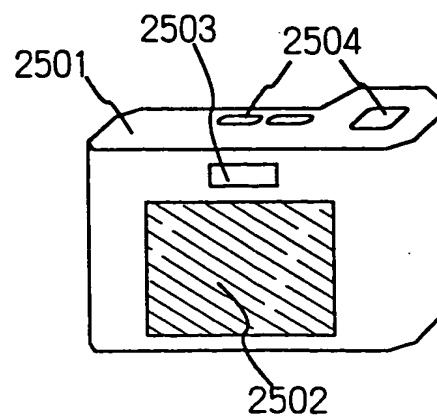


Fig. 11F

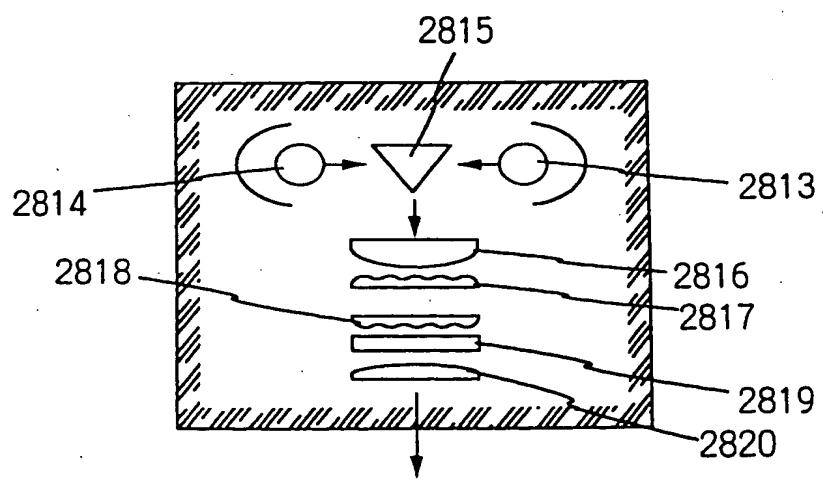
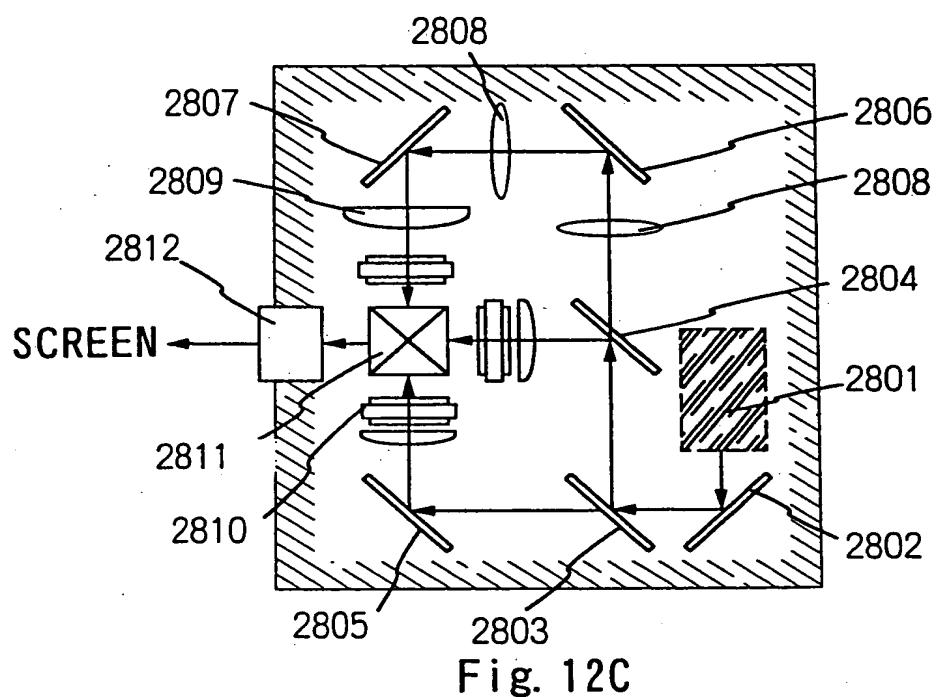
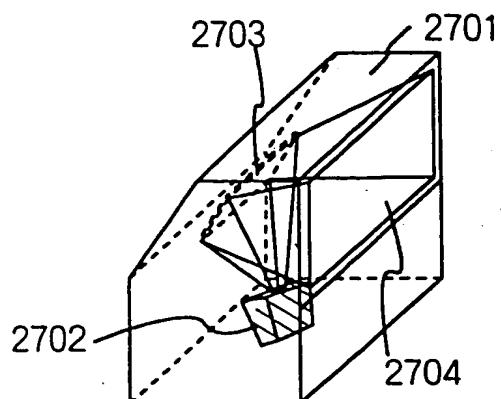
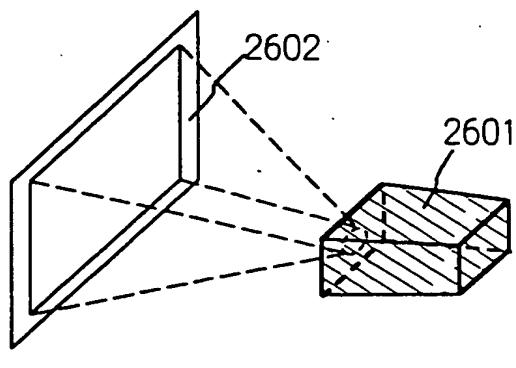


Fig. 13

